

Tech Talk

Fine Lines in High Yield (Part CXLVIII)

Adhesion to Copper - Trends and Issues

Karl H. Dietz (for CircuiTree Magazine, January, 2008)



Karl Dietz is the manager at DuPont's Electronic Materials Laboratory, Research Triangle Park, NC. His responsibilities include application studies for printed circuit materials. Karl has 35 years of experience in a variety of R&D, manufacturing and quality control functions and holds a PhD. in organic chemistry from the University of Frankfurt, Germany. If you would like to participate in the exchange or if you have any questions, Karl Dietz can be reached at 919-248-5248, fax: (919) 248-5132, or via e-mail <Karl.h.dietz@usa.dupont.com>.

First and second level packaging has always wrestled with yield and electronic packaging reliability issues that are associated with low adhesion of the copper to an adjacent organic phase, be it the dielectric insulator, a permanent material, or photoresist, a consumable material. With the advent of copper and "Low Dk" dielectric in IC fabrication, related concerns are now also part of IC fabrication.

Historically, forming a rough copper surface for better mechanical adhesion was a popular remedy to overcome poor chemical adhesion. However, we will look at several converging technology drivers that demand smoother copper surfaces for high performance interconnect structures, a trend that demands new material and process solutions.

We can list several copper adhesion issues in substrate and circuit board fabrication:

- The adhesion of the ED (electro-deposited) copper foil (see Figure 1) of the copper-clad laminate to the dielectric core which has traditionally been addressed by a combination of topographical and chemical alteration of the foil surface facing the dielectric.
- The adhesion of the innerlayer copper circuits to the prepreg during multilayer lamination which was addressed by applying an oxide multilayer bonder conversion to the copper surface, and more recently, by bonders that rely on alternative chemistries.
- The adhesion of electroless copper to build-up microvia dielectric films in the semi-additive process (SAP) which was historically achieved by properly engineering the dielectric resin and the filler size and size distribution, and by a solvent swell and permanganate etch of the dielectric film surface.
- The adhesion of vendor copper, panel-plated copper and electroless copper to the photoresist which was addressed by copper surface preparation and resist compositions that gave good conformation, wetting, and acceptable chemical adhesion to such prepared copper surfaces.

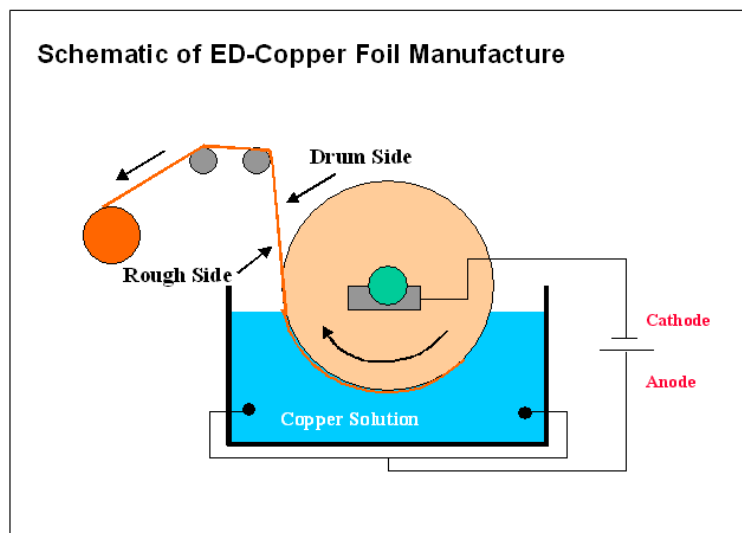


Figure 1: Schematic of ED-Copper Foil Manufacture



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The Copper Surface and Resist Adhesion

Copper might be considered an “almost noble metal.” Copper does not corrode as readily as iron, but it corrodes much faster than gold or platinum. Even freshly cleaned copper will show copper oxides and adsorbed water on the surface. As copper oxidizes, the metallic Cu⁰ first loses one electron, going to Cu⁺, then losing one more electron, going to Cu⁺⁺. The positive charges of the copper are balanced by the negative charges of oxygen in the oxide form (O⁻) or other negatively charged ions that the copper surface had been in contact with, such as chloride (Cl⁻), sulfate (SO₄⁻) or phosphate (PO₄⁻). Many surface cleaning issues have to do with removing excessive copper oxides (tarnish) or dealing with the removal of antioxidants (antitarnishes) that the laminate vendor has applied or which have been applied by the board fabricator at some step in the manufacturing process to preserve the copper surface long enough to stay “fresh” during a hold step in the process flow.

To understand some of the surface preparation issues it is useful to familiarize oneself with the composition and topography of standard ED foils and reverse treated foils (drum-side treated foils).

Figure 2 illustrates a fairly typical process for treating the rough side and smooth side of the ED foil. In a reel-to-reel continuous process the foil unwinds and passes through several treatments in a “Treater Line”. Copper dendrites are first grown on the rough side. These dendrites are brittle and need to be encapsulated in a second step with more ductile copper. This sequence is repeated, creating dendrites on top of dendrites. A zinc coating, or alternatively a brass coating, is then deposited, followed by the encapsulation with silane coupling agent which forms strong bonds with the resin.

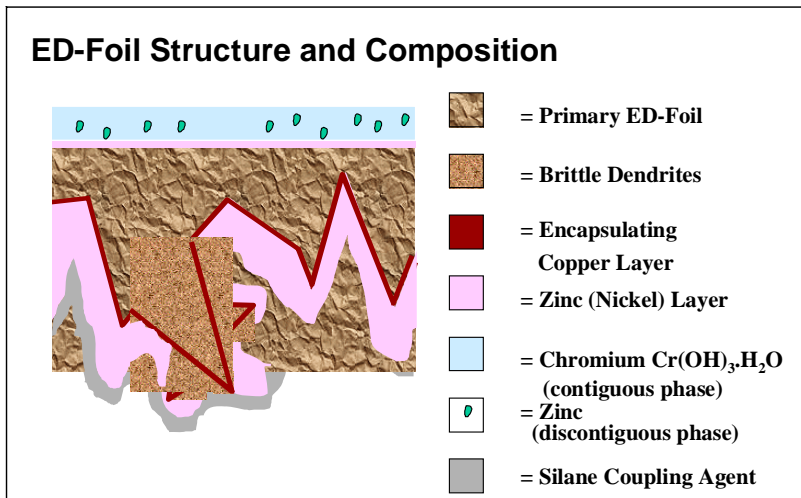


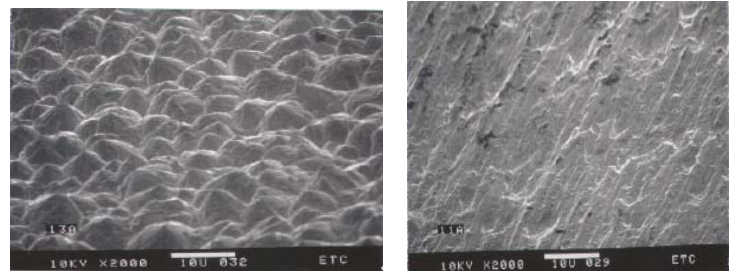
Figure 2: Example of an ED-Foil Structure and composition (not to scale)

On the smooth (drum) side, a very thin Zn(Ni) barrier is deposited, followed by a chromate/ zinc coating. The nickel barrier prevents the formation of copper/chrome intermetallics that are difficult to remove with acid cleaners. In the past, thickness and chemical composition of chromium layers were not well controlled and could lead to poor resist

adhesion and low yields. Great progress has been made in controlling the conversion coating. The desirable stainproofing properties are balanced against the ability to remove a fair portion of the chromium layer with a simple process step such as treatment with 10% sulfuric acid.

The “correct” chromate levels may be bracketed by qualitative tests which signal excessive or insufficient chromate levels see Tech Talk, Ref. 1).

Reverse Treated Foil vs. Standard Vendor Copper



Reverse Treated Foil (RTF)

Standard Vendor Copper

Figure 3: Comparison of Reverse Treated Foil and Standard Foil Topography

The chromated surface of the vendor copper is the surface to which the dry film resist is later applied after proper surface preparation. The chromate “conversion coating” serves as an antitarnish to preserve it and slow down the copper oxidation process. The “chromium” phase is actually a contiguous, hydrated Cr(OH)₃ phase, with chromium predominantly at the oxidation state Cr⁺⁺⁺, with interspersed zinc. The degree of hydration is critical to the removal of this layer in acid. Typical chromium coverage would be about 5mg/m².

Occasionally, vendors also apply organic antitarnishes such as benzotriazole. It is debatable why and to what extent these conversion coatings should be removed prior to lamination. In the case of chromate conversion coatings, there is ample evidence that most dry films do not adhere too well to such a surface. Also, in most innerlayer production processes, prelamination cleaning serves a dual purpose: the removal of chromate serves film adhesion, but is also necessary to assure good oxide formation for multilayer bonding.

Reverse Treated Foils (RTF)

As mentioned previously, the ED process creates a rough side that gets “treated” with zinc, or brass, and sometimes a silane coupling agent coating before this rough side is laminated to the dielectric. In the RTF process, the foil receives a zinc treatment only on the smooth (drum) side, which is laminated to the dielectric. Thus, RTF foil is sometimes referred to as “Drum Side Treated Foil” (DSTF). The rough, non-treated side faces the dry film. Because of its surface roughness, no mechanical or chemical roughening step is needed for dry film adhesion. However, since the roughness (Ra >0.3 micron) exceeds optimal topography for dry film conformation (see comparison

of standard foil with RTF in Fig. 3), best results are achieved under lamination conditions that improve conformation, e.g. with wet lamination, slower lamination speed, increased hot roll temperature, or added preheat. An acid cleaner is typically used for tarnish and chromate removal.

Trends towards Smoother Copper Surfaces Fine Line Etching

The practice of artwork compensation and over-etching in the print & etch process to achieve equal lines and spaces with more vertical circuit sidewalls works well if lines and spaces are not very small. It also serves another useful purpose. There is enough time in the etcher to assure the removal of copper “teeth” embedded in the dielectric resin. When etching very fine lines and spaces, over-etching is no more an option, and to avoid residual copper embedded in the dielectric space between circuits, so called “low profile” copper foil is being used.

The Use of Embedded, Planar Capacitors

Embedded planar capacitors are thin dielectric layers with copper foil on both sides that serve as power and ground planes. To achieve high capacitance density, it is desirable to keep the dielectric layer as thin as possible and have a high dielectric constant for which purpose fillers can be used. Very thin capacitor layers cannot tolerate rough copper because of the danger that the copper teeth in the dielectric may short out the capacitor or lower the breakdown voltage unacceptably.

The Use of Thin Core Innerlayers

Traditional copper surface preparation methods such as mechanical brushing, pumice or aluminum oxide treatments result in good copper micro-roughness for resist adhesion but can cause dimensional distortion of thin cores and are therefore not recommended. Instead, micro-etchants or acidic one-step cleaners that typically include some micro-etching are in use. The resulting topography has typically a lower roughness than is desirable for good dry film resist adhesion. There are several approaches to assure that the resist adheres to this smoother surface. Adhesion promoters in the resist formulation may be optimized for smoother copper surfaces. In addition, the resist can be made more hydrophobic. As a result, the resist will swell less in the developer, thus lowering the stress at the resist/copper interface.

Chemistry suppliers are offering chemistries that change the chemical composition of the copper surface for better adhesion to the resist, such as Atotech’s “ResistAssist”. The company Schmid (www.schmid-online.de, Ref. 2) has introduced inline equipment with atmospheric plasma to clean the surface of copper-clad laminate and activate it for better dry film adhesion.

Very Fine Line Circuitry Formed on Flip-chip Substrate Build-up Dielectric Layers

The adhesion of electroless copper to build-up microvia dielectric films in the semi-additive process (SAP) has traditionally been achieved by properly engineering the dielectric resin and the filler size and size distribution, and by a solvent swell and permanganate etch of the dielectric film surface (see process sequence of Figure 4).

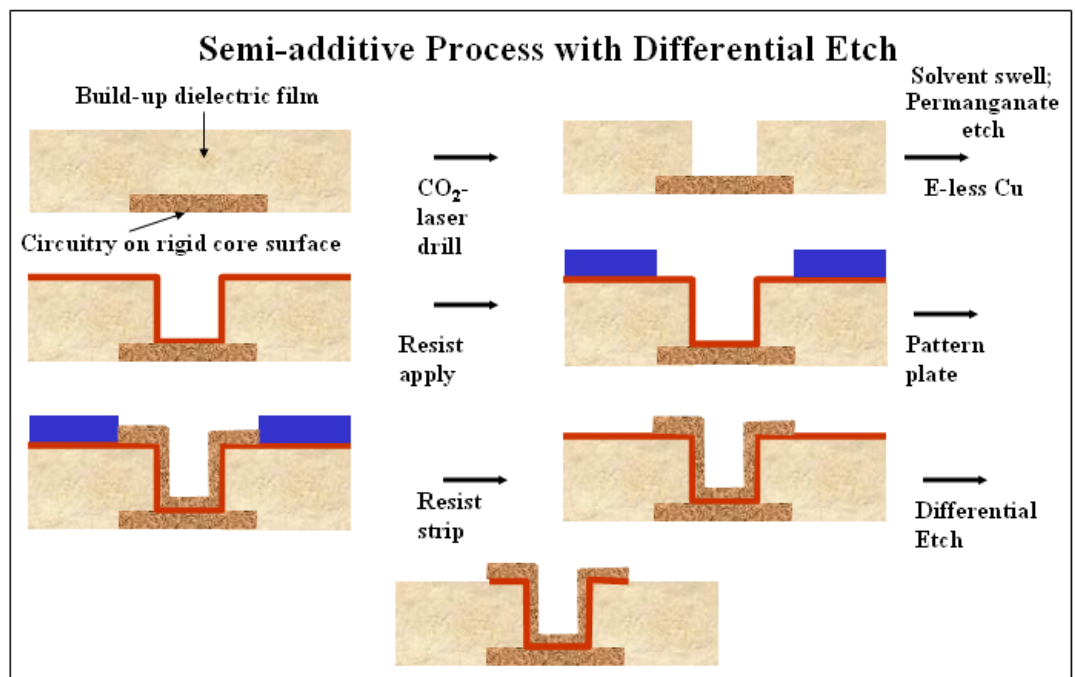


Figure 4: Semi-additive Process Sequence

The dielectric film typically showed a roughness of $R_a = 0.8$ to 1.0 micron after surface preparation due to the 1-2 micron diameter filler size and the size of the resin domains which etch at different speeds with permanganate. Reasonable copper peel strength (about 1 kN/m) could be obtained with such a surface roughness. However, to achieve 10 micron L/S for 2008 package and 8 micron L/S for 2012 as projected by the ITRS Roadmap surface roughness needs to be reduced for a number of reasons while copper peel strength needs to remain reasonably high (probably in the 0.6 to 0.8 kN/m range). The ITRS Roadmap only gives “state-of-the art” copper peel strength of 1.6 kN/m , but does not elaborate about an acceptable trade-off adhesion strength, nor does it mention a numerical value for low surface roughness that needs to come with 10 micron L/S. Fabricators who will supply future high performance substrates assume that an R_a of 0.5 or less will be required. The “critical to quality” (CTQ) flow down diagram of Figure 5 illustrates the cause and effect relationships that lead to the need for very fine lines and smooth copper.

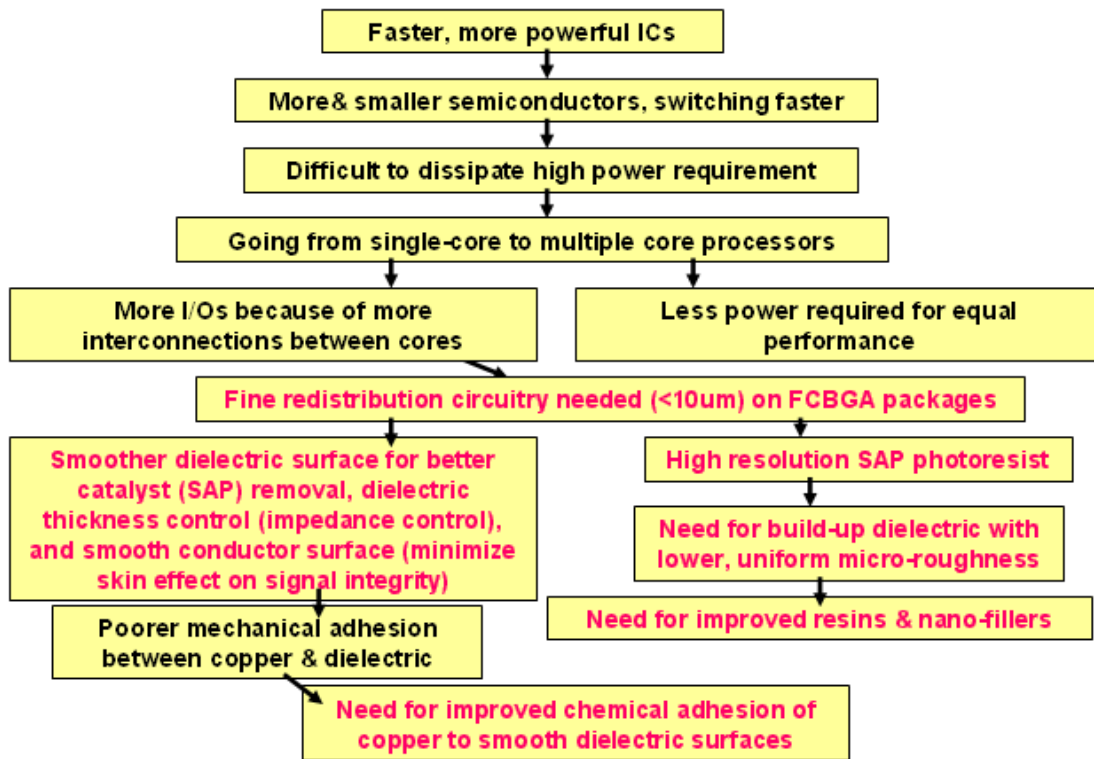


Figure 5: Drivers Leading to the Need for Finer Circuits and Smoother Copper

There are several considerations that favor smooth copper for fine circuits in high performance flip chip packages. One has to keep in mind that it is the surface roughness of the dielectric build-up film which is mirrored in the surface of the electroless copper. First and foremost, there is the concern that palladium seed particles remaining embedded in the rough dielectric surface of the narrow dielectric spacing between conductors may be a cause for shorts. To assure removal, a smoother dielectric surface is desirable. A second consideration is impedance control. A rough dielectric surface means that the height of the dielectric under the copper varies which in turn varies the impedance. And thirdly, at high frequencies the skin effect is more dominant. This effect refers to the phenomenon that the electric signal travels predominantly at the surface of the copper as opposed to the bulk of the conductor. If the copper surface is rough, the high frequency signal will get attenuated and will lose transmission speed.

In summary, there are several trends in electronic packaging that lead to the need for smoother copper surfaces, and as a consequence, impact materials and processes.

References

1. Fine Lines in High Yields, (Part XXIV): What About the Chromate on the Copper (Part B), Karl H. Dietz, CircuiTree Magazine, August 1997, pg. 64
2. Gebr. Schmid GmbH & Co, D-72250 Freudenstadt, Germany; e-mail info@schmid-online.de