Tech Talk

Fine Lines in High Yield (Part CXXV)

Fine Lines – Beyond the Limits of Semi-additive Processing?

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The finest circuitry in electronic packaging is found in the build-up microvia layers of IC packages. These circuits are formed by semi-additive processing (SAP, see Figure 1) which means a resist pattern is formed on top of very thin electroless copper, the circuits are then plated up, resist is stripped, and the base copper is "differential etched". This etching is done without a metal-etch resist to protect the plated copper and therefore some of the plated copper is lost as well. This means the resist pattern has to compensate for this etch-back. To form 10µm lines and spaces, the resist dimensions may be more like 8˜m wide resist lines and 12µm resist spaces, because the etching of the 0.5 to 1µm thin base copper will etch-back at least 1µm from both sides of the plated line. For a copper height of 12-13µm, this means that the resist needs to be about 15µm thick which results in a resist aspect ratio of about 2 to 1. This is tricky! The 8µm wide resist line does not have much of an anchoring surface to hold it in place during development and etching. There are more strikes against the SAP process at sub-10µm feature sizes.

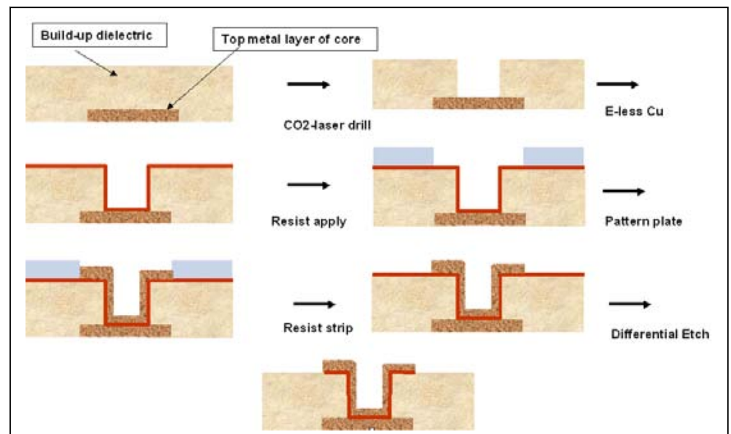

Fig.1: Semi-additive Process with Differential Etch

For a 20µm wide SAP-plated line, R. Watanabe (Ref. 1) reports about 5-6µm under-etch from both sides at the electroless copper/ SAP-plated interface, leaving only about 9µm anchoring surface for the copper line. This under-

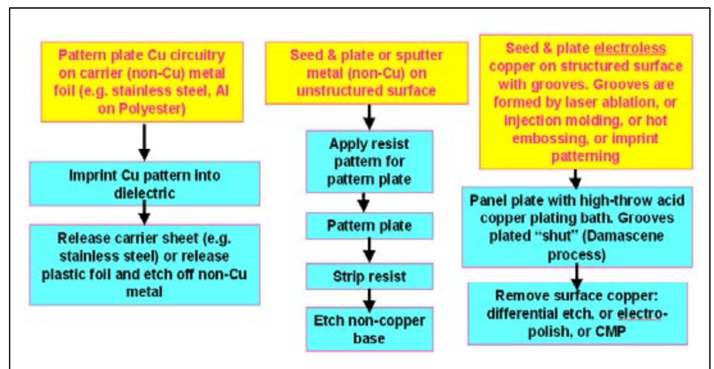

Fig. 2: Concepts for Fine Line Circuitization

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etch is in addition to the bulk-etch-back of the plated line suggesting that the interface between the electroless copper and the plated line is more susceptible to etchant attack. The reduction of the anchoring surface for plated copper will of course be an even greater problem for sub-10µm features. But this is not the end of the bad news yet: today's SAP process relies to a large extent on mechanical bonding of the electroless copper to the dielectric surface which has a roughness R_a in the range of 0.7 to 1µm. In the future, lower R_a values (about 0.2-0.5˜m) will be required to reduce the skin effect at high frequencies and to control impedance as build-up layer dielectric thickness is projected to go from 35µm to about 20µm. Therefore, copper adhesion to the dielectric will become a big problem.

It is conceivable that the SAP process can be extended to finer lines and spaces if the thin base metal is not copper. In such a case the base can be etched with an etchant that does not attack the copper, thus avoiding the etch-back (see Fig. 2, process flow in the middle). For example, chromium could be etched with permanganate, or aluminum with caustic. A more elegant solution would be to move away from raised circuit lines to embedded or recessed lines (see Fig. 3). Such recessed lines don't offer any surfaces to lateral shear forces, and instead of one anchoring surface they have three anchoring surfaces.

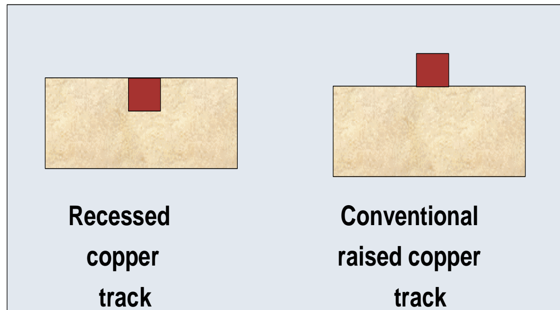

Figure 3: Raised vs Recessed Circuits

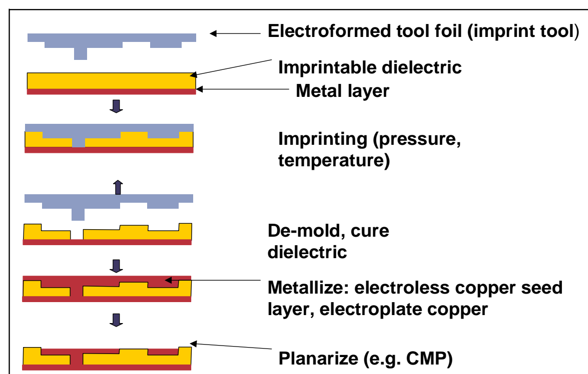

Fig.4: Principle of Imprint Technology (source: George Gregoire, Dimensional Imprint Technology, Inc.)

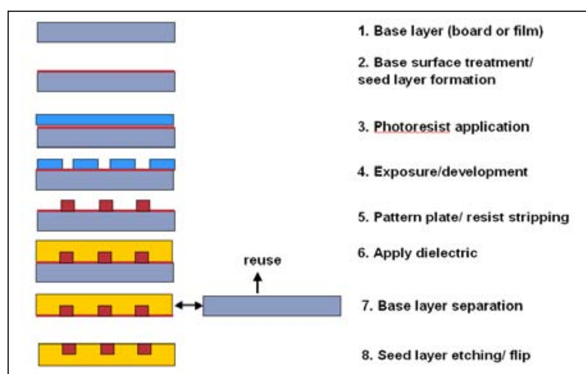

Fig.5 : Illustration of a Circuit Transfer Process (Source: Ryoichi Watanabe, Samsung Electro Mechanics, Ref. 1)

There are two basic ways to form recessed copper features, both of which have several variations on the theme (see Fig. 2). One concept consists of creating groves and holes in a dielectric to define the dimensions of conductor traces and vias. Groves and holes may be formed e.g. by imprint technology (see Figure 4, Ref. 2, 3), or hot embossing, or laser ablation. The other concept consists of forming circuit patterns "off-line" by pattern plating on a conductive layer (see Figure 5). This layer could be a metal seed layer on a non-conductive board or film (Ref. 4). An example might be a polyester base sputtered with aluminum. Or the conductive layer could be a stainless steel plate (Ref. 5).

It is not clear to me at this time which of these approaches has the most merit and will eventually emerge as the technology leader, or if an altogether different ciruitization method will prevail. It is however clear that a good number of progressive fabricators and OEMs are investigating these technologies.

References

1. New Circuit Formation Technology for High Density PWB, Ryoichi Watanabe, Samsung Electro Mechanics, Proceedings, S34-2, Electronic Circuits World Convention 10, Feb. 22-24, 2005, Anaheim, CA.)
2. "Imprint Patterning: A Novel and Possibly Disruptive HDI Option," George Gregoire, *The Board Authority*, September 2001, pg. 40.
3. "Innovative Uses Imprinted U-Shaped PWB Traces and Microvias," G. Gregoire, IPC Printed Circuits Expo, Proceedings S 01-1, April 1998.
4. Nikkei net interactive (www.nni.nikkei.co.jp): June 28, 2005 press release about CMK's process for manufacturing "ultra-smooth printed wiring boards" US Patent 4,606,787 (1986), Peter Pellegrino