Tech Talk

Fine Lines in High Yield (Part CXXVI)

Troubleshooting the PWB Fabrication Process

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Process engineers in charge of increasing the overall yield of a PWB fabrication process need the tools to track yield trends and to assign probable cause to defect types. Without such tools any process change intended to improve yields would be a stab in the dark. The effectiveness to improve yields of any process change could not be measured. "Yield by AOI" inspection is a common way to track innerlayer yields. Basically, the AOI compares the actual board with a perfect board ("golden board") and applies programmed pass/fail criteria to any observed deviation ("event") of the actual circuit pattern from the perfect pattern to distinguish between good boards and scrap. A deviation from the perfect board in simplistic terms is either copper in a non-copper area or no copper where copper should be. Examples are "opens", shorts", space violations (i.e. copper protrusions into the dielectric spacing), line width violations (i.e. less than full copper line width, "mouse bite"), copper spots ("extraneous copper", "copper splash", "dish down" (i.e. less than full copper height) etc. For "near opens" or "near shorts" an acceptable % of a feature size deviation from the nominal size needs to be programmed (e.g. 30% line width reduction is acceptable, but more than 30% is not). AOI operators often get a chance to assign the proper defect code, e.g. is the defect a line width reduction, or a dish down, or both. The AOI tool thus allows to calculate (first pass) yield, track yields by lot or shift, assign defect type description, and track relative abundance of defect types, e.g. 80% shorts, 10% space violations, 5% extraneous copper, and 5% line width violation. In this example our process engineer would be well advised to check into possible causes of under-etching.

Most AOI software packages don't have the capability to assign defect x/y coordinates, create defect maps of individual panels, and superimpose such defect maps of several panels from one lot or multiple lots to create composite defect maps. Such capability would be very helpful in distinguishing major categories of defect types: repeat defects, random defects, and patterns of defects that may lead to a probable cause. Dick Olson (Ref. 1) describes the use of composite defect maps in connection with a single pitch (e.g. 3 mil L/S) test board. To detect repeat defects one has to teach the software that creates the composite defect maps how much "slop" in x/y coordinate position one is willing to accept and still call a cluster of multiple defects "repeat defects". Repeat defects nearly always point to problems with the exposure process such as a faulty phototool, or the contamination on a phototool, or some other obstacle in the exposure light path.

Defect patterns that show up in composite defect maps are most useful to assign probable cause. For example, an abundance of opens near the leading edge of the panel may point to a tack-down bar problem in the cut sheet laminator. Or a streak of opens in machine direction may be due to mechanical damage to the resist in the developer caused by the transport system. Or a streak of shorts in machine direction may point to plugged nozzles in the etcher.

A single pitch test board, completely covered with quadrants of repeating line and space patterns is better suited to detect "random" defects (and repeat defects) than an actual production board.

The actual production board has less circuitry and therefore yields less data, and its circuit pattern is not random, nor is it always “single pitch”. Islands of fine pitch circuitry will attract higher defect counts than areas of coarser pitch circuitry, and areas without circuitry will of course show no defects, with the possible exception of “copper splash”. For these reasons, a real production board will never show a true random defect pattern.

If the AOI does not have the capability to create composite defect maps, one can resort to a poor man’s version of this tool by using a polyester foil (e.g. a blank phototool base) and mark on it the defect locations of multiple panels. This is a tedious and time consuming job but it can yield valuable insight.

Once repeat defects have been identified, troubleshooting of these defects is relatively easy. One should however be aware of so called “pseudo repeat defects” which can complicate troubleshooting. For example, a resist particle may be stuck on the phototool, causing repeat defects for a while until the particle is dislodged and all is well again.
Troubleshooting random defects is much more complicated. Randomness can be often associated with contamination. The problem is that there are multiple steps in the PWB fabrication process sequence where contamination can occur, and therefore we need a methodology that allows us to distinguish between contamination that occurs in surface preparation, exposure, development, or etching etc..

Troubleshooting the source contamination involves skipping certain processing steps. For example, to verify that the surface of copper-clad base material is free from contaminants such as epoxy spots, copper-clad base material is “blank”-etched. If no copper spots are detected after etching, one could conclude that the copper surface was free from contamination that could act as an etch resist. Of course, if the contaminant spot is very small the etchant could completely under-etch the spot and no copper is detectable after etching. Since the board had not been processed through drilling, surface preparation, lamination, exposure, and development, none of these steps can be implicated as sources of contamination.

To assess if drilling contributes to contamination, a drilled board is blank-etched. Any increase in unwanted copper after blank-etching vs the blank-etched un-drilled board is attributed to drilling. One would check in particular for copper around the drilled hole due to resin smear.

The next test could be blank-etching of the board after surface preparation. An example of contamination of the copper surface due to surface preparation might be nylon smear due to an insufficiently cooled brush.

If the next step in the processing sequence is the direct metallization of the through-holes, blank-etching before electroless copper might detect residual seed particles such as carbon or graphite on the copper surface.

To check for contamination during exposure, resist is laminated to copper-clad laminate and the resist is blank-exposed. Then develop, etch, and strip. Inspect for pin holes in the copper. Pin holes are an indication of contamination during exposure, blocking light, causing spots of non-exposure, causing development in these areas, and copper pin hole etching.

To check for contamination during development, and possibly during etching, laminate resist to base material, do not expose, then process through develop, etch, strip. A copper spot indicates the trapping of a contaminant on the surface of the copper during develop or etch that acts like an etch resist. An example might be a resist particle that was transferred from a roller to the copper surface, or “etcher goo” re-deposited to the board surface in the etcher. Such goo may have formed because of high acid normality attacking the resist.

Reference:

1. “What’s so hard about raising yields?”, Dick Olson, CircuiTree Magazine, March 2001, pg. 82