Tech Talk

Fine Lines in High Yield (Part CXXVIII)

HDI Trends and Developments

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Traditional HDI (high density interconnect) structures feature microvias in so called build-up layers. The microvias in adjacent build-up layers are off-set, or "staggered". Coreless structures, such as the ALIVH process can form staggered as well as "stacked" microvias. In addition to the ALIVH stacked microvia structures (Matsushita, see Figure 1), there are other stacked microvia processes such as the PALAP process (Denso, see Figure 2) and the FVSS process (Ibiden, see Figure 3) that are gaining traction in commercial applications. The ALIVH process has been a long time favorite in Japanese cell phone boards. The PALAP process is now robust enough that it will be used in navigation systems for some Toyota cars, and Ibiden will begin producing FVSS boards for cell phones in its new factory in Beijing in 2006. Stacked via processes are so popular because the combination of stacked and staggered vias enables designers to connect two points on different layers with the shortest conductive path which reduces inductance losses and electrical discontinuities.

Many OEMs that design cell phones such as Nokia and Sony Ericsson have decided to use bromine-free dielectrics even though brominated bisphenol A based resins have not been legislated away yet like other bromine containing compounds such as polybrominated biphenylethers. The trend to laser drillable prepreg (LDP) is continuing but RCC is still widely used. LDP has the reputation of being more reliable than RCC since the reinforcement lowers the CTE of the dielectric which reduces CTE mismatch at material interfaces and thus is less likely to cause cracks. However, new lead-free compatible dielectrics may not necessarily behave in the same manner and have to be subjected to the customary reliability tests.

The circuit density for cell phone boards (75˜m L/S, going to 50˜m L/S) is such that there is no need to switch to SAP (semi-additive processing) which requires a dielectric film such as Ajinomoto's ABF. Advanced HDI cell phone boards use a "modified" SAP process that uses copper foil which is typically thinned by an etching step. Specialized equipment such as the Songtex Technology Company Ltd (Taiwan) "Half-Etching M/C" and chemistry based on hydrogen peroxide are now available to perform this copper thinning. CO_2- laser drilling through thinned, surface-oxidized copper is becoming very popular because of the excellent registration of this process. The dark surface enhances the absorption of the laser energy.

The conventional way to laser drill with CO_2- lasers is to use the copper as "conformal mask". Holes are etched into the copper foil using print & etch technology. The holes define the size and location of the CO_2- laser drilled vias. This process has the typical registration problems that accrue due to phototool size changes, side-to-side registration tolerances, and etch variability. Registration is improved if the CAD drill data for the CO_2- laser define the hole location. In this process, the CO_2- laser is used to drill through thin copper as well as dielectric. An X-ray drill can first locate targets on the capture pad layer, then drill pilot holes to guide the CO_2- laser. If the capture pad layer has shifted, the CAD data for the CO_2- laser can be scaled, just like an LDI image. UV-laser drilling is catching up with CO_2-laser drilling as UV-lasers are becoming competitive in throughput with CO_2- laser drilling of very small diameter holes, and because the resulting holes are cleaner than a CO_2- laser drilled small hole. UV laser drills from Mitsubishi Electric Corp. and Hitachi Via Mechanics are popular. Hitachi Via Mechanics introduced the world's first, high speed 4-beam UV Laser Drilling Machine. It can drill 2000 holes/sec (through resin, such as Ajinomoto's ABF), enabled by Hitachi's new original Galvano and Top Hat optical system.

There is special AOI equipment for the inspection of microvias, e.g. Machvision's Laser-via AOIM, with a high speed scanning system that requires only about two minutes per panel to check for hole position, hole shape quality, evidence of drill wander, and cleanliness of the copper capture pad.

Electroplated copper via fill is becoming the prominent z-axis metallization for stacked and staggered vias in HDI. Atotech, Rohm & Haas, Uyemura and others have introduced special via fill plating processes. Organic additive systems for such plating processes had to be modified to improve the throwing power. Air sparging has been shown to give poorer results than impingement plating. The effect of current density on via filling parallels the experience with plated through-holes. The effect of the copper concentration, on the other hand, seems counterintuitive: the high-throw acid copper plating baths were developed from conventional bath by increasing the acid concentration and lowering the copper concentration. However, higher copper concentrations seem to improve via filling, an observation that suggests a plating mechanism limited in a way that is different from traditional PTH plating.

Laser direct imaging (LDI) appears to become more popular with HDI as image scaling allows better registration, and the depth of focus of the laser beam enables fine line lithography even if multiple build-up sequences cause slight non-planarity of the resist surface.

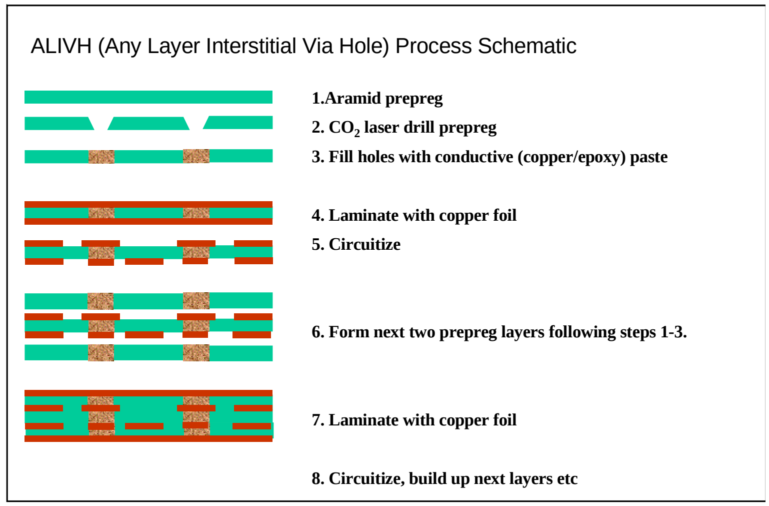

Figure 1: ALIVH Process Flow

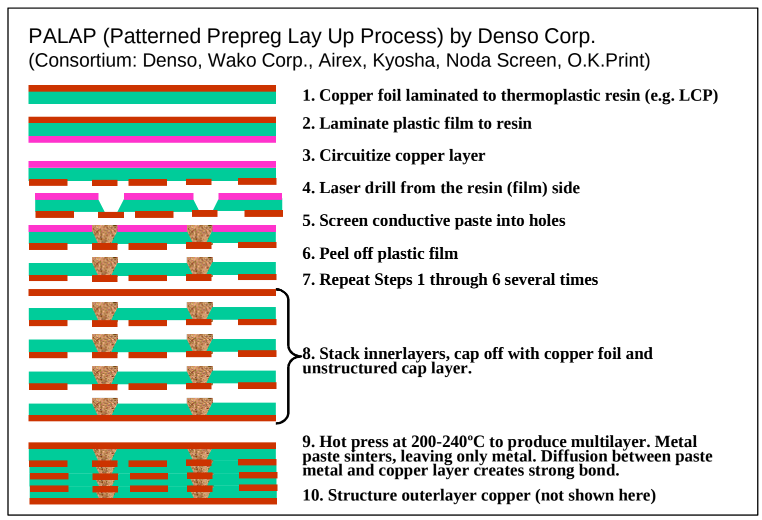

Figure 2: PALAP Process Flow

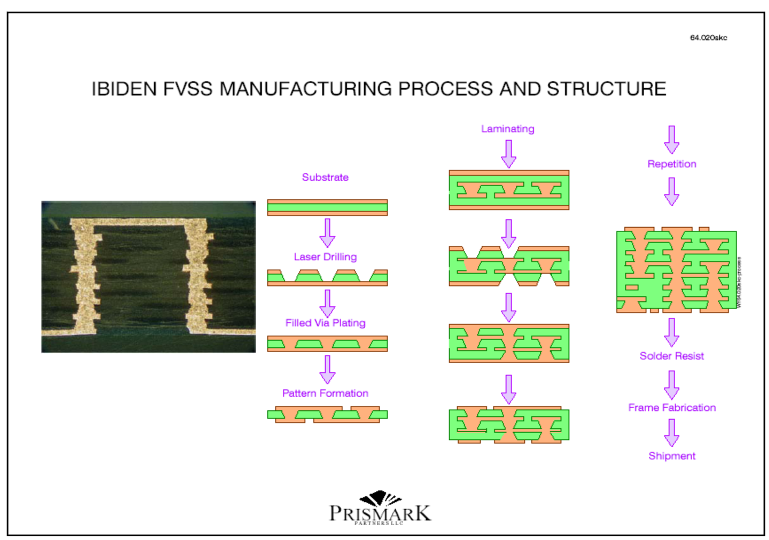

Figure 3: FVSS Process Flow (source: Prismark)