Tech Talk

Fine Lines in High Yield (Part CLIV)

Advances in Copper Plating (Part A)

Karl H. Dietz (for CircuiTree Magazine, July, 2008)

Karl Dietz is the development manager at DuPont's Electronic Materials Laboratory, Research Triangle Park, NC. His responsibilities include application studies for printed circuit materials. Karl has 35 years of experience in a variety of R&D, manufacturing and quality control functions and holds a PhD. in organic chemistry from the University of Frankfurt, Germany. If you would like to participate in the exchange or if you have any questions, Karl Dietz can be reached at 919-248-5248, fax: (919) 248-5132, or via e-mail <Karl.h.dietz@usa.dupont.com>.

It was at the IEEE Symposium on VLSI Circuits (Honolulu, Hawaii, 2004) when Shekhar Borkar (Director of Circuit Research for Microprocessors, Intel) voiced the opinion the he doesn't see anything to replace copper. This remark referred to the use of copper in IC fabrication, in first and second level packaging, and not to long distance data transmission. Copper is displacing aluminum in IC fabrication, copper pillars are competing with solder bumps, new plating processes and plating bath compositions allow to plate micro-vias "shut" in a bottom-up via-fill process and enable the metallization of TSVs (through silicon vias). Extensive studies have shed light on the role of plating additives and other parameters that play a role in these via fill processes. In addition, there have been advances in the rejuvenation of plating baths and in recycling of rinse waters from plating operations.

Environmental Advances

It was found that traditional methods to remove organic contaminants from acid copper plating baths, such as active carbon or a combination of active carbon and hydrogen peroxide, gave unsatisfactory results with periodic reverse pulsed plating baths so that the throwing power of the bath and the metallurgical properties of the copper deposit deteriorated with time. A new UV oxidation process (Enviolet®, Ref. 1) is removing organic contaminants more effectively as was demonstrated by TOC (total organic carbon) and HPLC (high performance liquid chromatography) analyses. Sulfur containing compounds are oxidized by this process to sulfate and organics are converted to CO_2 or highly oxidized compounds that are electrochemically inactive. The UV radiation forms OH radicals from hydrogen peroxide which abstract hydrogen radicals from organic compounds that then react with oxygen to form peroxides which further oxidize to CO_2. This method was found effective in rejuvenating or waste treating other plating baths, e.g. the removal of ETDA from spent electroless copper plating baths.

Reference 2 describes a novel method for recycling rinse water from copper plating operations using electrical remediation. The system integrates electrowinning and ion-exchange to remove copper and reduce TDS (total dissolved solids). The electrical remediation uses a forward pulsed waveform.

"Bottom-up" Via-fill Processes

These processes can be used to create stacked vias in HDI boards and IC substrates. Added advantages include improved planarity, better thermal conductivity of the vias, and the ability to place solder bumps directly on top of a microvia connection. This via fill technology can not only be applied to blind microvias but also for filling through-holes as reported by Ref. 3.

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Using conventional plating baths and plating parameters, copper deposits faster on the board surface than in through-holes and blind vias, and vias show the familiar "dog bone" shaped copper thickness distribution. So it is puzzling that there are conditions under which more copper is deposited in the hole than on the surface and vias can be filled from the bottom up.

Early on in the development of via fill plating processes it was found that the type of agitation, the copper to acid ratio, the current density, and the microvia aspect ratio all had an influence on the plating quality. Figure 1 shows the beneficial effect of impingement-type bath agitation. Figure 2 shows the effect of the copper concentration and current density on via filling. Figure 3 shows how the microvia aspect ratio, or via diameter for a given height, affects the percentage filled. Uziel Landau and others studied the mechanism by which

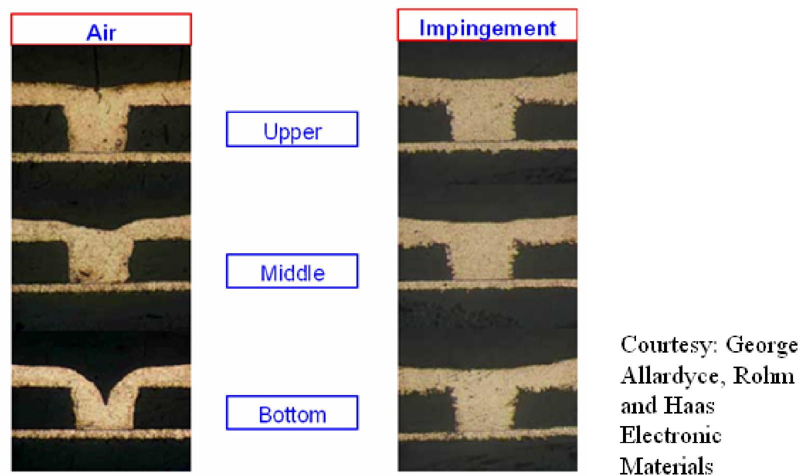


Figure 1: Air Sparging vs Jet Impingement

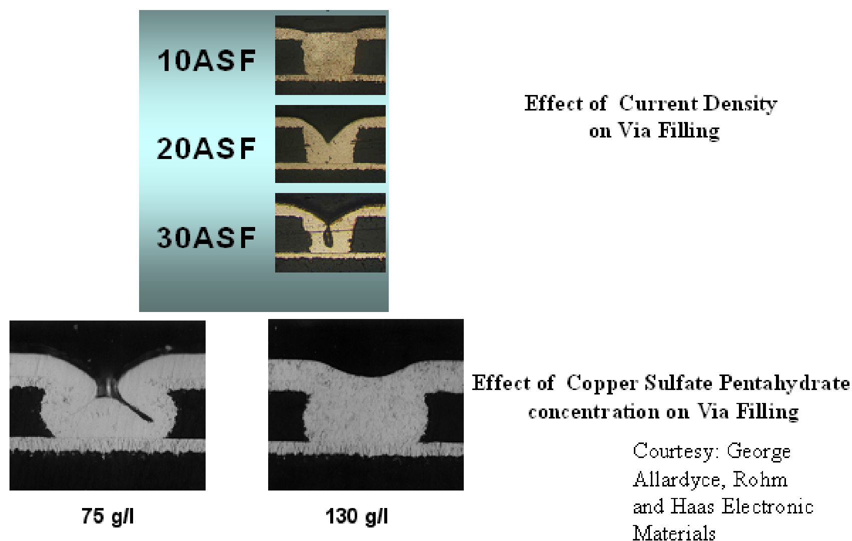


Figure 2: Effects of Copper Concentration and Current Density

plating additives enable “bottom up” plating (Ref. 4, 5, see also Ref. 6).

The functions of plating additives are fairly well understood (Ref.7, 8): polyglycols such as polyethyleneglycol (PEG) act as inhibitors, small amounts of chloride enhance the inhibiting effect of PEG, bis(3-sulfopropyl)-disodium-sulfonate (SPS), other disulfides, thiourea, thiocarbamates act as accelerators, and quaternary nitrogen compounds act as levelers. Landau studied in particular the role of PEG and SPS in the bottom-up via fill process. He points out that at the beginning of the plating process there are hardly any additives in the via hole to be adsorbed on the hole wall and hole bottom surfaces because of the low liquid volume to surface area ratio in the via. PEG adsorbs faster than SPS but there is very little PEG to cover the hole walls and bottom. However, on the surface, the PEG supply is plentiful and the fast adsorbing PEG inhibits plating on the surface. In contrast, practically all additives that end up on the hole surfaces have to diffuse into the hole. Since SPS diffuses faster than PEG, it reaches the bottom of the hole first, and once adsorbed, forms a barrier against PEG adsorption. The slower diffusing PEG slowly builds up on the upper part of the hole wall near the surface, acting as a plating inhibitor while the dominant SPS at the bottom of the hole accelerates plating. See Figure 4 which illustrates the additives distribution as a function of via depth position very early in the plating cycle. The red spheres symbolize SPS and the green spheres symbolize PEG. Landau found that the relative concentrations of PEG and SPS have an influence on how well the bottom-up plating

Via Filling (MCP-PAL)

Material:RCC

Plating Thickness: 25um

Current Density: 20 ASF

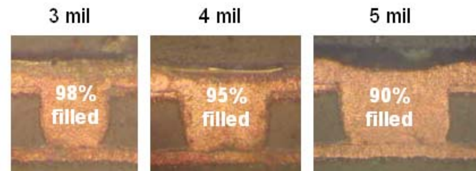


Figure 3: Effect of Via Aspect Ratio (Source: PAL)

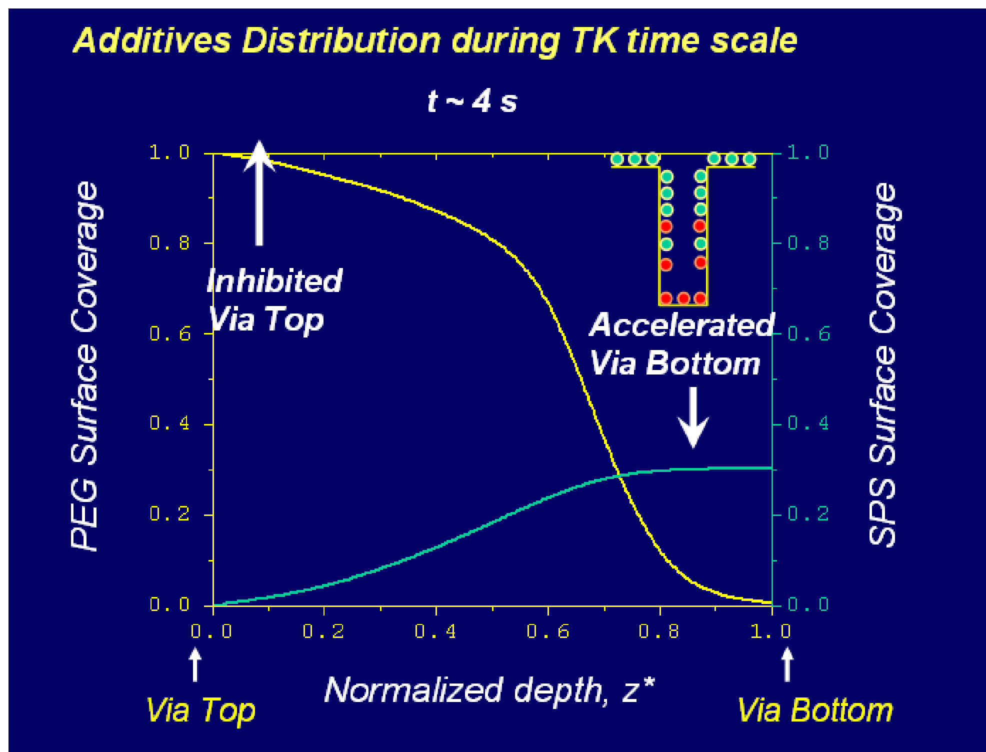
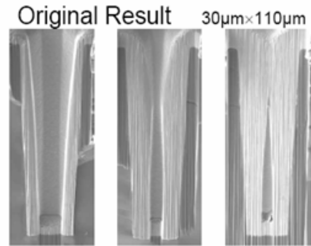


Figure 4: Additives Distribution in a Blind Via (courtesy U. Landau)

Through-Silicon Vias (TSV)

TSVs enable the z-axis interconnection of 3D die stacks. There are several TSV processes, typically distinguished by the processing sequence ("via first" and "via last" processes) and by the conductive interconnect material used such as polysilicon, tungsten, or copper. The copper is electroplated into a very high aspect ratio blind via that is either etched or laser drilled into the wafer and covered with a seed layer. After "bottom-up" via fill plating, the wafer is back-ground to the bottom of the blind via to expose the copper. The via fill plating performance is influenced by a number of factors (Ref. 9). A non-optimized plating bath resulted in current crowding near the via opening and premature closing at the top of the via, leaving a void (see Fig. 5). After optimizing the plating bath composition and the waveform much improved results were obtained.



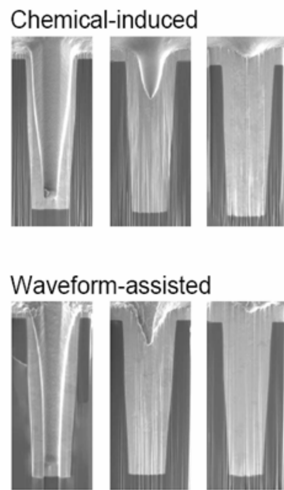


Figure 5: Improvements in "Bottom-up" Plating by Bath Composition and Waveform Selection
(Source: Bioh Kim, Semitool)

performs. His findings also explain the effect of via diameter and aspect ratio on the bottom-up plating performance (see Figure 3). Wider via diameters mean a less favorable volume to area ratio in the hole which means there is more PEG initially available to adsorb on the via bottom. A high aspect ratio via results in a greater concentration gradient in the hole cylinder between a slowly diffusing additive such as PEG and a faster diffusing additive such as SPS, thus favoring bottom-up plating.

The challenge is void-free plating without reducing the current density unduly so that productivity is maintained.

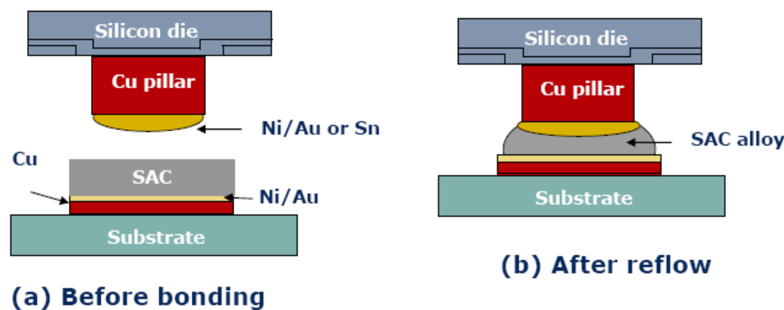


Figure 6: Schematic of a Copper Pillar Interconnection (source: Mark Huang, Micron)

Copper Pillar Plating

Wafers are typically bumped by plating solder, stenciling solder or solder ball placement. These techniques all involve a reflow step that results in a sphere-shaped bump so that for a given, desired stand-off height the pitch will be limited since the bumps are basically as wide as they are high. Copper pillars, on the other hand, are plated, capped with tin, nickel/gold, or tin/silver, but don't go through a reflow process so that they remain pillar shaped and allow finer pitch (Ref. 10, and Fig. 6). Copper pillars also have the added advantage of better thermal and electrical conductivity.

Electropolishing

Electropolishing is of course the opposite of plating and one could argue that it does not belong in an article on plating. Electropolishing is the electrochemical removal (or de-plating or corrosion) of metal from a metal surface that forms the anode of a cell whereby metal is removed faster from surface protrusions than from valleys so that the result is a smoother surface. R. Venkatachalam (Ref. 11) has shown that surfaces get even smoother if a pulsated direct current is employed. In recent studies, M. Buhlert and others have found that this method can further be refined by selecting specific impulse times and current densities as well as specific pulse frequencies (Ref. 12).

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