

EMBEDDED CERAMIC CAPACITORS: THE ROAD TO RELIABILITY

Diptarka Majumdar, John Summers, Richard Traylor, Olga Renovales

DuPont Electronic Technologies
14 T. W. Alexander Drive
Research Triangle Park, NC 27709
Email/Ph: Diptarka.Majumdar@usa.dupont.com /919 248 5134

ABSTRACT

Technology development for embedding of passive components has been the subject of significant focus for OEMs, board fabs and material suppliers for the past few years. This has been driven primarily by the need to miniaturize portable devices like mobile phones though performance advantages accruing from embedding passives is also becoming increasingly significant.

DuPont's focus in the area of Embedded Passives has been on the development of resistive and capacitive materials for applications in organic substrates. The product family includes a wide range of materials viz. ceramic and polymer thick-film capacitor and resistor pastes for discrete embedded devices and filled and unfilled organic laminates for applications requiring planar capacitance. Previous publications have described the technology development involving standard thick-film and printed wiring boards (PWB) processes to embed thick-film ceramic passives in PWBs. This paper focuses on reliability of embedded thick film ceramic capacitors.

INTRODUCTION

Current commercially available embedded passive materials include etchable thin film resistor laminates, organic capacitor laminates, and polymer thick-film capacitors and resistors. The capabilities and limitations of existing technologies have been discussed in the literature.¹⁻⁶

The embedded ceramic capacitor technology, which is the subject of discussion in this paper, is based on a combination of two well-understood commercial processes: nitrogen-fired thick-film hybrid production and traditional printed circuit board fabrication. Despite a few inherent incompatibilities between the two processes, a robust and viable process has been developed through significant innovation to enable the embedding of discrete ceramic capacitors in finished organic substrates. Along with the benefits accruing from embedding capacitors, this also affords the possibility of achieving much higher capacitance density than can be achieved with non-ceramic materials.

A key technology hurdle that had to be overcome for embedded ceramic capacitors to be deemed as commercially acceptable was to meet performance standards for the high humidity and bias test (HHBT, 85% RH, 85 C, 5V DC). This paper discusses the work done to develop materials and their application to enable embedded capacitors to successfully meet HHBT performance standards.

NOMENCLATURE

Thick-film, ceramic, embedded capacitors, organic substrates, hydrophobic polymer, insulation resistance (IR), thermal cycling test (TCT), breakdown voltage (BDV), high humidity and bias test (HHBT).

THE PROCESS

The process flow for embedding ceramic capacitors has been documented quite extensively elsewhere⁷. In brief, it combines conventional thick film processing and standard PWB (printed wiring board) processes to address a pivotal need of modern electronic designs. Key issues pertaining to the thick film and PWB sections of the process flow have been addressed over the past few years to develop a robust manufacturing process for bare substrates.

SUBSTRATE DESIGN

The placement of embedded discrete passives in a PWB substrate is dictated by considerations of manufacturing cost and electrical performance and design among others. Generally speaking, two broad variations in device placement are possible viz.

- (i) devices placed on an outermost layer (layer 1 and/or layer N of a N layer board) as in Figure 1a
- (ii) devices fully embedded in the substrate (layer 2 to layer N-1) as in Figure 1b

Test designs have been fabricated with FR4 and BT prepreps. Designs with and without cores (e.g. BT-HL832 HS) have also been tested.

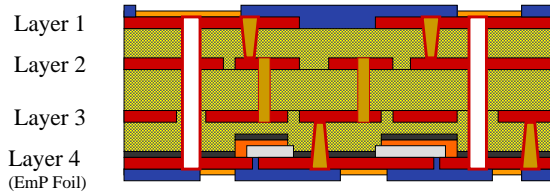


Figure 1a – Schematic showing embedded passives on outermost layer of PWB

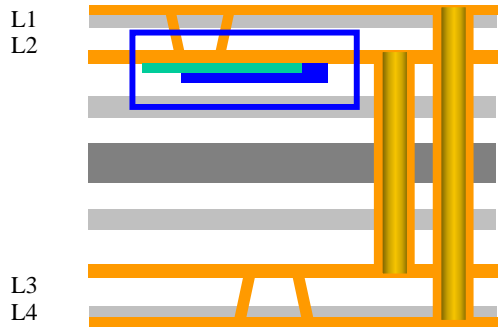


Figure 1b – Schematic showing passives placed on layer 2 of a multilayer PWB substrate

RELIABILITY OF EMBEDDED CERAMIC CAPACITORS

As a potential substitute for surface mount capacitors, embedded ceramic capacitors are expected to meet the relevant reliability performance standards specified for their surface mount counterparts⁸.

Some key reliability performance standards that embedded capacitors have to meet are listed in Table 1. Internal testing had determined that the capacitors have acceptable endurance to

- (i) thermal cycling (TCT)
- (ii) breakdown voltage (BDV)
- (iii) temperature and humidity (TH)

However, the capacitors are not as robust when subjected to a DC bias along with exposure to temperature and humidity. Figure 2 shows degradation of insulation resistance in capacitors located on layer 2 of a 4 layer PWB (Figure 1b).

<i>Test</i>	<i>Performance Spec</i>
Breakdown Voltage	various
Temperature / Humidity : Moisture Absorption, 85C/85%RH, with bias	1000 hrs without IR failure, < 15% drift in capacitance
Thermal Cycle (air to air), - 55C to +125C	1000 cycles without IR failure, < 15% drift in capacitance, -40C to 125C

Table 1 –Key reliability parameters and associated performance metrics for embedded ceramic capacitors

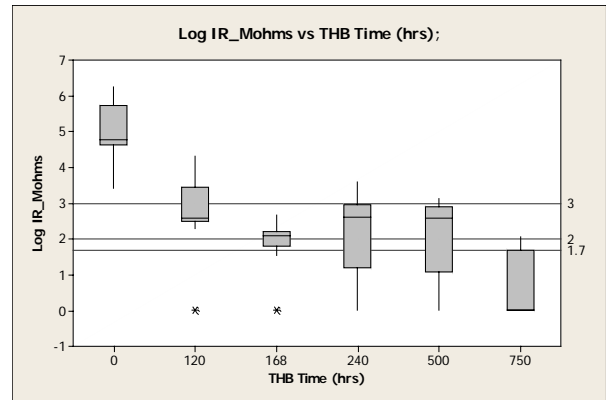


Figure 2 – IR degradation of embedded ceramic capacitors in bare substrate on exposure to HHBT (85C/85% RH, 5V DC bias)

Table 2 shows the processing conditions for capacitors on foil which were embedded in the PWB stack shown in Figure 1b and evaluated against the reliability performance standards listed in Table 1. As described in an earlier publication⁷, the preprint is a thin layer of a copper thick film paste which is screen printed on a copper foil preceding the deposition of the capacitor dielectric. In some cases the preprint is fired before printing of the dielectric (prefired) while in others it may be fired along with the dielectric (cofired).

<i>Panel ID</i>	<i>Preprint</i>	<i>Lamination P (psi)</i>
B1	prefired	450 (traditional)
B6	no preprint	450 (traditional)
B1_screen	prefired	450 (traditional)

Table 2 – Processing conditions for embedded capacitors used for reliability evaluations

(i) Thermal Cycling Test (TCT)

Figure 3a shows thermal cycling (-40C to 125C, air-to-air) data for embedded ceramic capacitors for which the preprint was prefired (B1 in Table 2). After 500 hours,

the maximum deviation in capacitance observed was well within 15%. Further testing up to 1000 hours was discontinued due to the excellent thermal cycling stability exhibited at 500 hours.

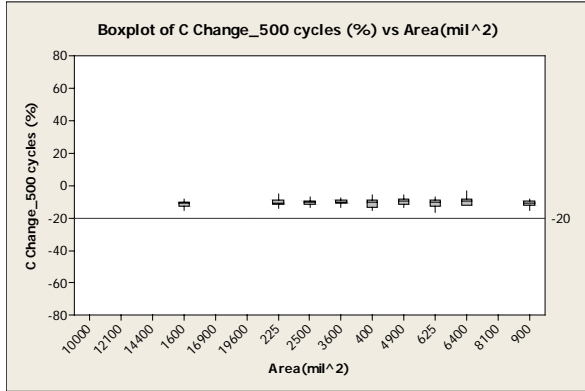


Figure 3a – TCT data for capacitors ranging in size from 15 mil to 80 mil square

(ii) Breakdown Voltage (BDV)

Unlike performance in TCT, the results of the breakdown voltage test were strongly impacted by capacitor area with larger capacitors exhibiting lower BDV (Figure 3b). However, mean BDV even for capacitors as large as 120 mil square was greater than 150 V.

Figure 3c shows the effect of preprint on BDV for 80 mil square capacitors. For the given population, the use of a preprint increased mean BDV from 300V to almost 400V.

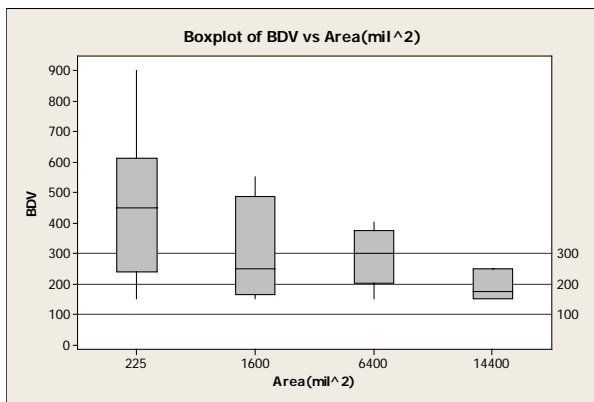


Figure 3b – Mean BDV as a function of active area of embedded capacitor

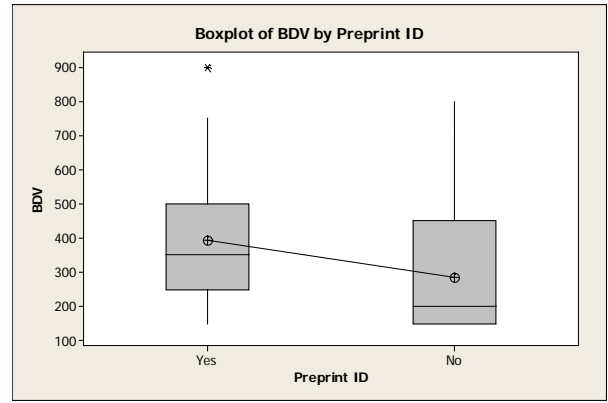


Figure 3c – Effect of “preprint” on mean BDV of embedded capacitors

(iii) Temperature and Humidity Test

Capacitors embedded in boards were exposed to 85C at 85% relative humidity and their capacitance and insulation resistance monitored over 1000 hours. Irrespective of size, there was very little change in capacitance over the course of the test. The maximum change in capacitance recorded was about 5% (Figure 3d). Insulation resistance of the capacitors measured at 100V DC for 15s did not degrade.

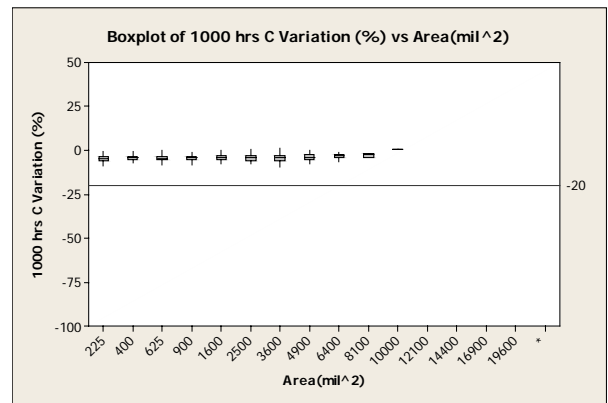


Figure 3d – Capacitance drift over 1000 hours in TH (85C/85% RH)

However, when the same capacitors were subjected to a 5V DC bias at 85C/85% RH, the insulation resistance degraded precipitously in the first 100 hours of testing and dropped below a threshold value of 50 Mohm beyond 500 hours (Figure 2). The capacitance continued to be robust with little or no change observed over 1000 hours (Figure 3e).

Mechanism of Capacitor Failure in HHT

Electrochemical compromise of capacitor dielectrics in the presence of moisture and applied voltage is well

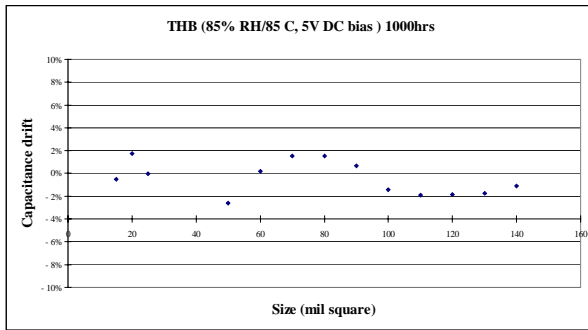


Figure 3e – Capacitance of embedded ceramic capacitors is robust to temperature, humidity and DC bias

known. Broadly speaking, it consists of the following steps.

- (i) ingress of moisture into the dielectric body
- (ii) adsorption and condensation of water molecules on the pore walls of the dielectric
- (iii) solvation of ionic species and available ionic contaminants on the pore walls
- (iv) transport of dissolved ionic species between the capacitor electrodes under applied voltage to form a leakage current that is sufficiently large to instantaneously dissipate stored charge thereby resulting in a loss of insulation resistance

Solution to the HHBT Problem

The active nature (constituted of ionic species) required of the capacitor dielectric for storage of charge does not lend itself to a solution to the HHBT problem through a tailoring of the dielectric composition itself. Therefore, it was decided that the most appropriate solution should aim to eliminate the ingress of moisture into the capacitors in the first place. Based on this technical approach, we developed a proprietary resin composition loaded with inorganic fillers to “encapsulate” the capacitors and thus act as a protective cover or barrier against moisture. Significant amount of work was done to address processing issues associated with developing a polymeric composition which after curing would be impermeable enough to moisture to allow the embedded capacitors to meet HHBT performance standards.

Encapsulant Development

The following attributes were selected as goals for encapsulant development:

- Defect-free screen printability over 10-40 μm thickness

- Ability to fill or seal surface and microstructural defects in the dielectric
- Cross-linking chemistry that is stable at room temperature but takes place in a reasonable time under mild curing schedules
- Very low water uptake to effectively protect the dielectric from moisture, especially when the capacitor is under bias in a humid environment
- Good adhesion to various materials used in PWB construction, including FR4 type substrates, solder mask, fired electrodes, and the dielectric itself
- Chemical resistance to strong acids, bases, and other compounds encountered in typical PWB process flows
- Low levels of ionic contamination
- A combination of modulus and thermal expansion coefficient that does not impart significant stress on the dielectric and/or the capacitor assembly that is encapsulated

Composition

Several commercially available resins were scouted along with several resins from the siloxane family. These were proven to be inadequate in fulfilling one or more of the criteria above. However, through careful selection of resins, a formulation that inherently possessed very low water uptake, good chemical resistance, good adhesion, and compatible cross-linking chemistry was identified.

Rheology and Screen Printing

An inorganic filler was added to the resin formulation modify the printing characteristics of the paste and to tailor the mechanical properties of the cured encapsulant. Other modifiers were added to the paste in small amounts to optimize paste printing characteristics to ensure defect-free coverage of capacitors.

Curing

The formulation can be cured by exposing it to 190C for 30 minutes.

Endurance to Wet PWB Chemistries

Encapsulated capacitors were prepared on ceramic coupons and exposed to concentrated acidic and basic solutions for 5 minutes. Specifically, 30% sulfuric acid and 30% sodium hydroxide were used. The capacitance, dissipation factor, and insulation resistance of the encapsulated capacitors were measured before and after exposure. Typical data of a robust encapsulant are summarized in Table 3 below.

Property	Initial Value	Post Dip Value	
		Acid	Base
capacitance (pF)	42.1	43.2	42.6
dissipation factor (%)	1.4	1.3	1.3
insulation resistance (Gohm)	5.1	4.8	4.4

Table 3 – Corrosion resistance data showing good endurance of encapsulant to exposure to strongly acidic and alkaline chemistries

The data reveals that this particular encapsulant is resistant to strongly acidic and basic conditions encountered in typical oxide treatments and is therefore capable of protecting the underlying capacitor from the corrosive effects of these chemicals. By comparison, unencapsulated capacitors fail this test.

Corrosion Resistance

The integrity of an encapsulant candidate was evaluated electrochemically by exposing an encapsulant-coated copper foil to a 3% sodium chloride solution at 60°C for 20 hours under a 3V bias. An AC impedance measurement was taken every 1.5 hours during the test. Results for a particular encapsulant cured under different conditions are shown in Figure 4a below. The corrosion resistance of all coatings was very high, even after several hours of exposure to 3% NaCl at 3V DC bias.

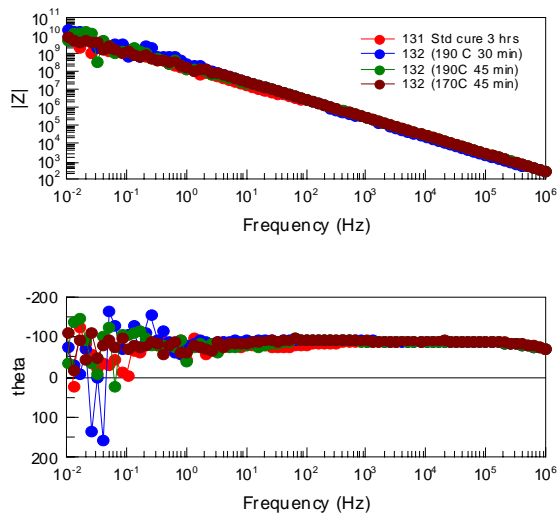


Figure 4a – Corrosion resistance of encapsulant to 3% NaCl at 3V DC bias

Endurance to Moisture

Candidates were also evaluated by preparing capacitors using the encapsulant as the dielectric. Then, these capacitors were aged under 85/85 conditions while exposing them to 5V DC bias to quantify the ability of the encapsulant to resist moisture uptake under these conditions. The insulation resistance was monitored during the test. If the IR declined significantly, this was a sign that moisture was penetrating the encapsulant and was generally viewed as undesirable. As a reference, unencapsulated capacitors fail this test within a few hours. Figure 4b below summarizes the performance of an encapsulant that successfully retained its performance characteristics during the course of the test. The insulation resistance remained high, indicating the encapsulant was an excellent moisture barrier.

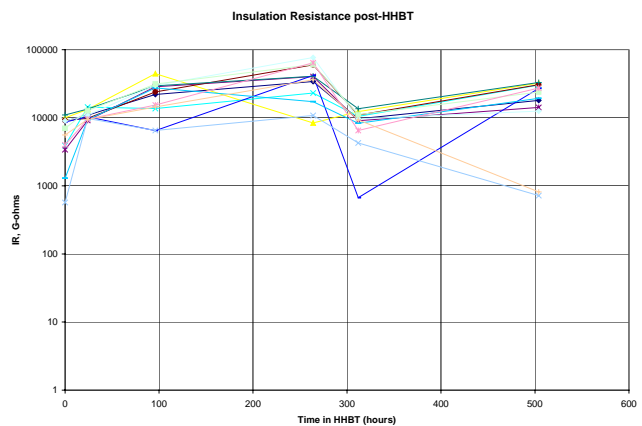


Figure 4b – Insulation resistance of cured encapsulant post-exposure to 85C/85% RH at 5V DC

Demonstration of Robustness in HHBT

Printed circuit boards with embedded ceramic capacitors were fabricated to demonstrate the effectiveness of the developed encapsulant as a moisture barrier. A simple PWB design (Figures 5a and 5b) was deliberately chosen to eliminate extraneous factors from impacting HHBT performance and therefore allow evaluation of the effectiveness of the encapsulant as a moisture barrier for the dielectric.

A 4-layer board construction was used with the ceramic capacitors residing on L2. An innerlayer comprising L2/L3 was made and laminated with layers 1 and 4. 1oz. NT-TOI copper foils from Circuit Foil Trading Inc. were used for layer 2. The TOI foil is a single side Zn-free treated electrodeposited foil and is designed to provide high bond strength on a wide range of organic substrates. Consequently, the innerlayer with the capacitors did not need to be subjected to an oxide process to ensure adequate adhesion to the 1080 FR4 prepreg used to build the boards. A low lamination pressure of 125 psi was used at both innerlayer and final lamination to avoid causing any mechanical damage to the ceramic capacitor. The capacitor height was roughly 30 μm and included 5

µm each of preprint and printed electrode and 20 µm of the ceramic dielectric. The two plies of FR4 in each layer were at ~150 µm in the finished boards.

The external finish on the boards was ENIG (electroless Ni/Au). All etching of copper was done with an alkaline etchant.

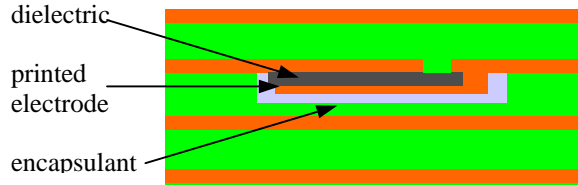


Figure 5a – Schematic x-section of board stack-up used to test encapsulated capacitors in HHBT

Figure 5b shows a slight variation on the theme of Figure 5a. In this case, the printed electrode completely envelops the ceramic dielectric and the active area of the capacitor is formed by etching the copper foil adjoining the capacitor. This proprietary capacitor design eliminates the possibility of cracking of the capacitor dielectric due to sintering stresses that inevitably arise during the firing of the capacitors in a hot wall furnace after they have been printed on the TOI foil. The designs in Figures 5a and 5b are also referred to as “standard” and “enveloping electrode” capacitor designs respectively.

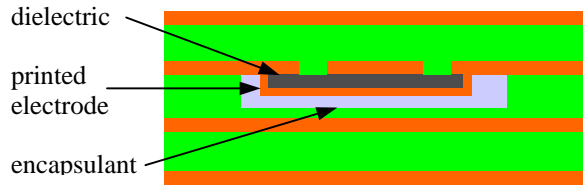


Figure 5b – Schematic x-section of board stack-up for HHBT test showing a printed electrode which completely envelops the capacitor dielectric

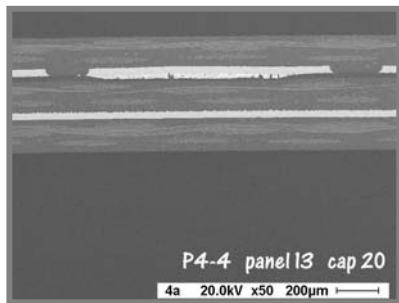


Figure 5c – Cross-sectional view of embedded capacitor with protective layer of encapsulant

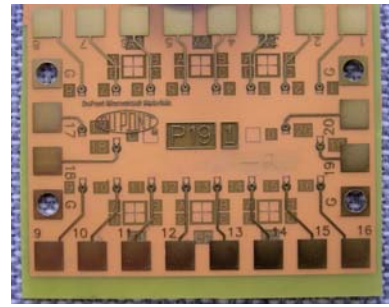


Figure 5d – Top view of finished module used for HHBT

HHBT Results

Figures 6a and 6b show the effect of HHBT conditions on the insulation resistance and capacitance respectively of embedded ceramic capacitors as a function of time. The other factors studied were capacitor design and the effect of a 10 µm encapsulant coating on the capacitor. Insulation resistance was measured with a LCR meter at 100V DC for 15s while capacitance was measured without any bias at 10 kHz.

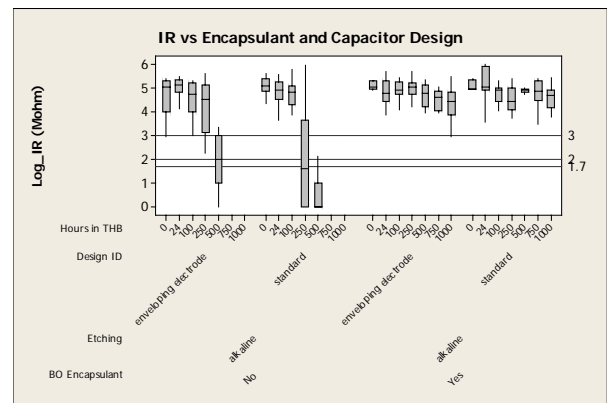


Figure 6a – Insulation Resistance data for different capacitor designs with and without encapsulant cover for protection from moisture in HHBT conditions

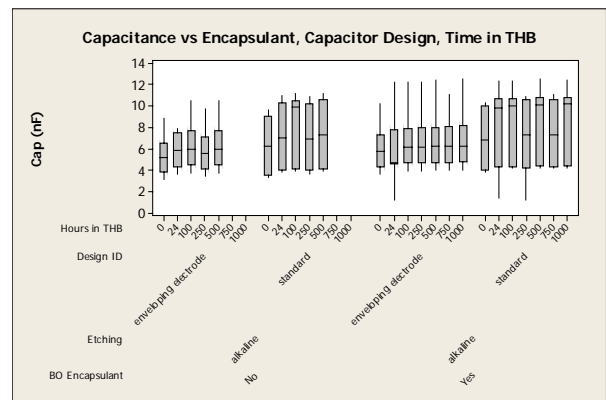


Figure 6b – Capacitance data for different capacitor designs with and without encapsulant cover for protection from moisture in HHBT conditions

The data indicates that the presence of the encapsulant allows the capacitors to survive 1000 hours in THB and is indispensable for guaranteeing reliability as indicated by the steady values for insulation resistance for encapsulated capacitors. The capacitors without encapsulant but with an “enveloping electrode” design also retain their initial insulation resistance values for a longer time than their “standard” design counterparts probably because the electrode provides a barrier to moisture permeation into the dielectric. It may be relevant to mention here that the “enveloping electrode” is 10 µm thick compared to the 5 µm thickness of the screen printed electrode in the “standard” design. However, the “enveloping electrode” is not as effective a moisture barrier as the encapsulant and the capacitors lose their insulation resistance after 500 hours of exposure to HHBT conditions.

Compared to insulation resistance, capacitance values are less sensitive to the combined stimuli of temperature, humidity and DC bias as seen by comparing Figures 6a and 6b. While all the capacitors with “standard” design and no encapsulant lost their insulation resistance at 750 hours, the capacitance distribution for the same population remained unchanged.

SUMMARY

The demonstration of the endurance of embedded ceramic capacitors in HHBT is a small step in the characterization of the thick film materials involved but a giant leap in the validation of the commercial viability of this technology. Despite the simple PWB designs and process flows used, this work has demonstrated that this technology matches the incumbent (MLCCs) in a key reliability performance. With the added benefits of elimination of solder joints, inventory, assembly and rework vis-a-vis their surface mounted counterparts, embedded ceramic capacitors provide a very convincing and compelling option

to meet the ever increasing need for miniaturization and improved performance in modern electronic designs.

ACKNOWLEDGMENTS

The authors gratefully acknowledge Dr. Suixin Zhang of Coretec Inc., Toronto for making the test boards, Richard Snogren of Bristlecone LLC for his help with PWB design and fabrication and the Embedded Passives team at DuPont Electronic Technologies for their contribution to this work.

REFERENCES

1. W. J. Borland and S. Ferguson, “Embedded Passive Components in Printed Wiring Boards: A Technology Review,” Circuitree, March 2001.
2. D. McGregor, “Standards Development Efforts for Embedded Passive Materials,” IPC Annual Meeting, October 2001.
3. P. Sandborn, B. Etienne, and D. Becker, “Analysis of the Cost of Embedded Passives in Printed Circuit Boards,” IPC Annual Meeting, October 2001.
4. J. Savic, R. T. Crosswell, A. Tungare, G. Dunn, T. Tang, R. Lempkowski, M. Zhang, and T. Lee, “Embedded Passives Technology Implementation in RF Applications,” IPC Expo, March 2002.
5. J. J. Felten and S. Ferguson “Embedded Ceramic Resistors and Capacitors in PWB -- Process and Design,” IPC Expo, March 2002.
6. AEPT website: www.aept.ncms.org
7. D. Majumdar, W. Borland, J.J. Felten and M. Doyle “Ceramic Embedded Passives for Organic Substrates”, Proceedings of IMAPS New England Chapter Annual Meeting, May 8, 2003, Boxboro, MA.
8. EIA-198-2-E MLCC Specifications, January 1998, Published by Electronic Industries Association, Arlington, VA, USA.