Decoupling of High Performance Semiconductors Using Embedded Capacitor Technology

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Abstract
The integration of embedded DuPont Thick Film capacitors and HiK polyimide based planar capacitor materials in IC packages has been investigated by a joint program initiated and sponsored by DuPont with the Georgia Institute of Technology Packaging Research Center (PRC). The PRC provided the build up multilayer fabrication and electrical modeling and simulation capabilities and DuPont provided the embedded passive component materials.

Test vehicles with different types of structures were designed, fabricated and tested for individual device characterization. The test vehicles included embedded ceramic-fired-on-foil capacitors with microvia interconnects and two sequential industry standard build-up layers on each side of a BT core. Feature sizes were 12 micron lines and spaces and 50 micron diameter microvias. Other test vehicles used a core layer without build-up layers, planar capacitor layers and arrays of discrete capacitors with different size, type and interconnection designs. Each capacitor variation was electrically characterized to select the preferred capacitor design having the best combination of properties and frequency performance. The electrical performance data from the test vehicles was used to create models of alternative package designs and to perform simulations to determine the designs offering the most effective power delivery and noise decoupling for a package having 2007 ITRS die and substrate features.

The embedded ceramic capacitors show a significant improvement in power system noise decoupling and charge supply to the IC versus existing surface mount solutions due to the low inductance design. The simulations used to compare the performance of the embedded capacitors versus using only surface mount capacitors in semiconductor packages show the capability to provide sufficient capacitance to meet the needs of Integrated Circuits dissipating 50 to 60 Watts.

Introduction
The International Roadmap for Semiconductors (ITRS) has projected an increase in the power consumption of microprocessors for future technology nodes [1]. Table 1 shows a variation of different microprocessor parameters for the 90, 65 and 45nm nodes. For example, for 2007 chips with a feature size of 65nm and a supply voltage of 0.9V, the power dissipation is projected to be 103.6 Watts. The power delivery network (PDN) provides the power supply to the processor. If improperly designed this network could be a major source of noise, such as ground bounce and electromagnetic interference (EMI). [2] A methodology for designing a good PDN is to define a target impedance for the network that should be met over a broad frequency band [3].

This parameter can be computed by assuming a 5% allowable ripple in the voltage supply and a 50% switching current in the rise and fall time of the processor clock [2]. Target impedance can then be calculated as:

$$Z_{target} = \frac{V_{dd} \times 0.05}{I \times 50\%},$$

where V_{dd} is the core voltage of the processor and I is the current drawn by the microprocessor from the PDN. The calculated target impedance for the 90, 65 and 45nm technology nodes is listed in Table 1. The current can be calculated from the power and voltage as:

$$P = V_{dd} I$$

Table 1: Target impedance through technology nodes

Year	Feature size (nm)	Power (W)	Vdd (V)	Current (A)	Target Impedance (mΩ)
2004	90	84	1.2	70	1.7
2007	65	103.6	0.9	115.11	0.7
2010	45	119	0.6	198.33	0.302

The decoupling capacitors play a very important role in the PDN as they act as charge providers for the switching circuits. The PDN target impedance has to be met over a broad frequency band; the low frequency, mid-frequency and high frequency capacitors need to be appropriately placed to meet this requirement. The performance of SMT capacitors is dependent on the loop inductance resulting from their placement on the substrate and their self-inductance. The inductance of the power ground plane affects low equivalent series inductance (ESL) high frequency capacitors more than high ESL low frequency capacitors. [4] This trend is further magnified in a decoupling capacitor network. The inductance of the SMT capacitor network dominates the response close to 100 - 300 MHz. Current SMT capacitors therefore provide good IC decoupling up to around 100 - 300MHz.

On-chip decoupling is practical for frequencies above about 2-3 GHz. Decoupling in the frequency range of between around 100-300 MHz and 2-3 GHz cannot be addressed by using on-chip capacitors, since the amount of on-chip capacitance that can be added is limited to the real estate on-chip. An increase in the amount of on-chip decoupling capacitance would prohibitively increase the cost and the size of the chip [5].

It is difficult, and some say impossible, to provide sufficient decoupling in this mid-frequency range of 200-300 MHz to 2-3 GHz. This presents a challenge to designers if they are to meet the impedance requirement over the entire frequency range

Research Program.

Working with the PRC a multi-phase program was defined to evaluate the mid-frequency performance of an IC package with embedded thick-film high capacitance discrete capacitors and HiK polyimide based planar capacitors. Due to the low inductance of embedded capacitors a significant improvement in power system noise decoupling and charge supply to the IC was expected over existing surface mount solutions. The goal of the program was to meet the 2007 Microprocessor technology requirements defined by the ITRS Technology Roadmap. [1]

Test vehicles with conservative design rules with different types of structures were designed, fabricated and tested for device characterization. The test vehicles included embedded fired ceramic-on-foil capacitors (capacitance density = 135nF/cm^2). The ceramic-on-foil capacitors were manufactured by DuPont using a methodology described elsewhere [7,8]. Connections were by microvia interconnects through two sequential industry standard Ajinomoto ABF layers on each side of an un-patterned Mitsubishi Gas & Chemical BT core. Feature sizes were 12 micron lines and spaces (L/S) and 50 micron diameter microvias. Other test vehicles used a core layer (no build-up layers), planar capacitor layers and arrays of discrete capacitors with different size, type and interconnection designs. Each capacitor variation was electrically characterized to obtain their real and imaginary components using a VNA 2-port measurement methodology to select the preferred capacitor design having the best combination of properties and frequency performance. The electrical performance data from the test vehicles was used to create models of alternative package designs and to then perform simulations to determine the designs offering the most effective power delivery and noise decoupling for a package using 2007 ITRS die and substrate features. The data was also used to perform a simulation to compare the performance of the embedded discrete capacitors with that of a substrate using only surface mount capacitors.

Capacitor Array Design Methodology

The characteristics of the individual capacitors were determined from the test vehicle data. Excellent correlation of model to measurement was achieved. Figure 1 is a package cross section with embedded capacitor layers and Figure 2 depicts a typical model to measurement result.

Figure 3 shows an embedded capacitor array layout. The purpose of the array network is to provide the decoupling from approximately 100-200 MHz to 2-3 GHz. To achieve this, different size capacitors were used in the array. The rationale for varied sized capacitors is that the impedance associated with each of them is different resulting in a range of resonant frequencies in the desired frequency range.

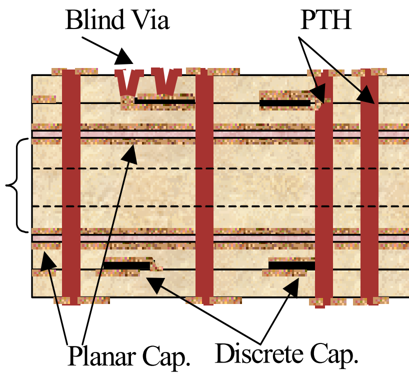

Figure 1. Cross section of package

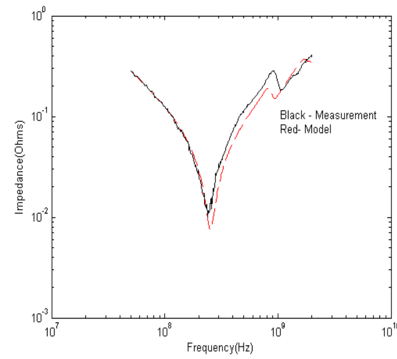

Figure 2. Model to measurement results of embedded capacitors

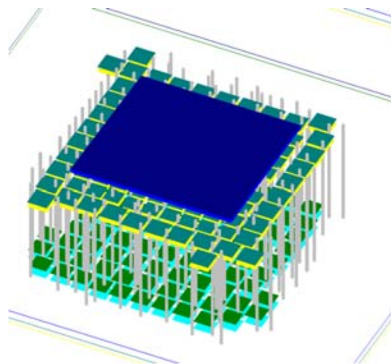

Figure 3. Schematic of an array of Discrete embedded capacitors

The vias and interconnections that connect the capacitors to the power / ground solder balls of the chip also influence the performance of the array. By proper co-design of the vias, capacitors and interconnections, the frequency band under consideration can be targeted. The capacitors are connected in parallel with each other to meet the target impedance. The number of capacitors required of a particular type is:

$$\frac{Z_{target}}{ESR_{cap}},$$

where ESR_{cap} is the equivalent series resistance of an individual capacitor. The capacitor frequency response is very sensitive to its position in the package. It is important to be able to place these low equivalent series inductance (ESL) capacitors in the "die shadow" of the processor. The die shadow is the area of the package projected under the footprint of the die, as viewed from the top. Placement of these capacitors outside the die shadow may cause routing problems and change the predicted performance of a capacitor because of increased inductance.

Simulation Models of Embedded Capacitor

For the frequency domain simulations the package structures were modeled using the GA Tech Transmission Matrix Method [6]. A single reference port in the structure was used which is the chip looking into the package. The package was assumed to be 4 cm by 4 cm. A package core dielectric thickness of 0.6 mm and copper thickness of 10 to 18 um for each layer was used. The flip-chip bump inductance and ball grid array (BGA) solder ball inductance was included in the model. The flip-chip bumps and solder balls were modeled using the GA Tech Fast Henry tool. For the chip to the package interface, the flip-chip bump diameter of 50um was assumed and a pitch of 213um was calculated based on 2007 ITRS requirements. The inductance of a single bump pair was calculated to be 16.45pH. In the 2007 65nm node, for 1024 bump pairs, the total effective inductance of the bumps is $1.6e^{-14}$H. Carrying out a similar analysis the inductance of a single supply BGA ball pair was calculated as 90.13pH. The diameter of the BGA ball and the pitch was assumed as 500um. For 500 such pairs the effective inductance is $1.80e^{-13}$H. Embedded capacitors within the package were used to target the mid-frequency band from 100MHz to 2GHz as previously discussed. Figure 4 compares the complete frequency response of the package using chip capacitors and embedded capacitors. The improvement in the frequency response with the use of a comparable number of embedded capacitors in the package can be clearly seen.

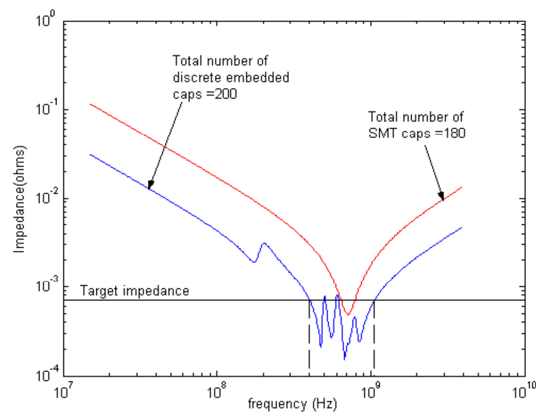

Figure 4. Improvement in Frequency response with Embedded capacitors

I/O Decoupling

To demonstrate the power supply noise improvement of discrete embedded capacitors versus that of SMT components a transient simulation of an I/O line was performed. A 1 GHz pulse train of rise and fall time of 100 psec was injected into a 70 Ohm microstrip transmission line. The voltage on the power supply was monitored with the RLC equivalent values for SMT and embedded discrete capacitors decoupling the power supply. The schematic of the simulation circuit is shown in Figure 5. The effect of the embedded decoupling capacitors can be clearly seen in Figure 6. With embedded capacitors the power supply noise is 0.05% as compared to 0.2% when SMT capacitors are used for decoupling. In addition to achieve comparable capacitance to the embedded capacitors used in this simulation required SMT capacitors using a much larger area. This clearly shows the benefit of embedded capacitors for I/O power supply noise reduction. The power supply fluctuation in these simulations is small, since it was assumed that only one driver is switching. In case of simultaneously switching drivers, the reduction in the power supply voltage fluctuation using embedded capacitors can become essential.

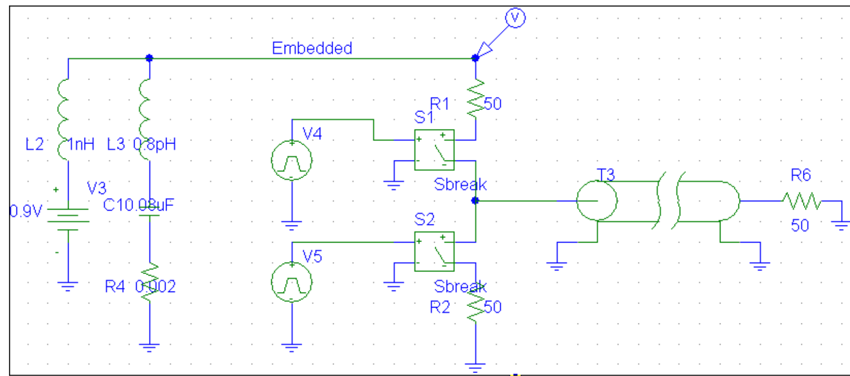

Figure 5. Schematic for the I/O decoupling simulation

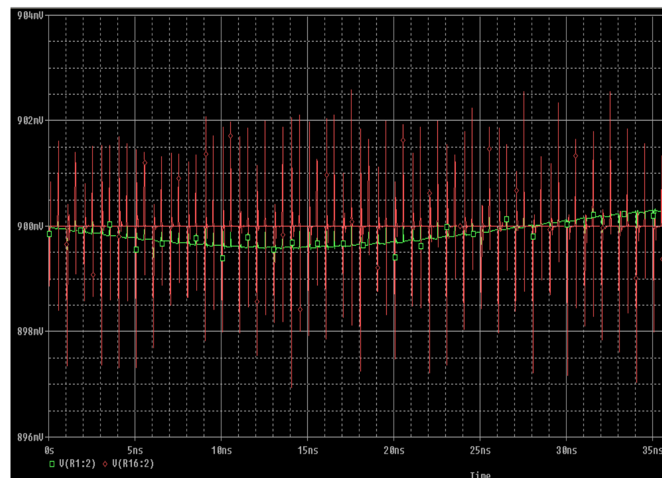

Figure 6. Simulation of power supply fluctuation

Power Dissipation

The amount of on-chip capacitance required that would maintain the required target impedance is determined by the frequency response of the decoupling networks in the package at 3 GHz. The architecture of a possible capacitor array in the package in a PDN designed to meet 2007 technology needs was simulated. Using conservative, proven design rules using the thick film embedded capacitors, the achievable impedance value was 4 milliohms. To determine the chip power dissipation that this design could support:

Achievable target impedance = 4 mohm
Core voltage = 0.9V
Current = 0.05V/ 0.5 X Z target = 22.5A
Power Dissipation = 22.5A X 0.9V = 20.25W

With modest improvements in the embedded capacitor designs to further reduce the target impedance it is projected that 50 to 60 Watt devices can be supported. Additional simulations were performed using advanced design rules where capacitors were designed closer together and with varying sizes resulting in high confidence that power dissipations on the order of 50-80 Watts can be effectively decoupled using the capacitance supplied by the thick-film capacitors (capacitance density = 135nF/cm^2). Figure 7 plots power levels vs. clock frequency typical of various classes of ICs and relates the appropriate capacitance density requirements using various designs for these ICs.

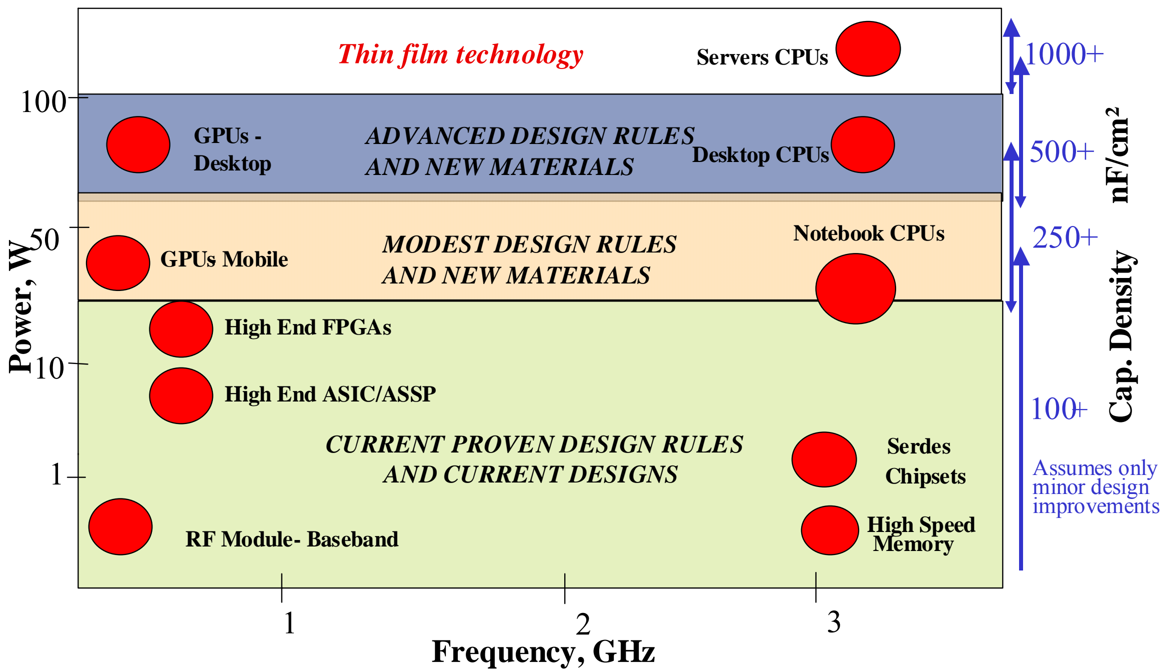

Figure. 7 Power, Frequency and Capacitance Density Needs

Conclusions

For decoupling in the mid frequency range of 100-300MHz to 2-3 GHz, embedded capacitors in the package have shown very good performance for low to medium power dissipation requirements. Embedding capacitors in the package positions them much closer to the chip reducing the inductance associated with the capacitor interconnections. Reduced inductance coupled with high capacitance significantly improves the decoupling performance. Thick-Film capacitor technology can address the "gray area" for decoupling in the mid-frequency range. For frequencies higher than about 2 to 3 GHz on-chip capacitors would be sufficient.

Using the current designs we have shown that thick-film embedded capacitors having a capacitance density of 135 nF/cm² can provide sufficient capacitance to meet the needs of IC's dissipating 20 watts. It was determined that for power dissipation in excess of 50 watts, improved design rules and higher capacitance density capacitors are needed

Acknowledgements

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